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Design of a Photovoltaic Grid-Tied Inverter Employing a Dual-Stage Boost Converter and a Transformer-Less Step-Down Circuit

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Abstract

This paper proposes a topology for a transformer-less, pure sine wave grid-tie inverter (GTI) for photovoltaic (PV) application. The proposed GTI employs a dual-stage boost converter, a transformer-less step down circuit, an H-bridge inverter and a T-LCL Immittance conversion circuit. The switching technique of the proposed inverter consists of a combination of sinusoidal pulse width modulation (SPWM) and a square wave along with grid synchronizing conditions. As the suggested method is entirely transformer-less, it significantly reduces the total harmonic distortion (THD) of the output voltage (less than 0.1%), minimizes its size and swells the inverter efficiency up to 97%. The T-LCL Immittance conversion circuit not only reduces the harmonics of the inverter output but also provides a nearly constant output current thereby stabilizing the system rapidly. The overall performance of the proposed inverter is simulated using PSIM using the designed values of circuit components. The simulation results show that the proposed inverter is capable of not only eliminating harmonics but is also highly efficient, compact and cost effective.

Keywords: Boost Converter, Step- down Circuit ,T-LCL Immittance Converter, Grid-Tie Inverter (GTI)

Introduction

The changing world climate is a serious threat to our planet. The global warming phenomenon, driven by the emission of carbon dioxide (CO2) from the use of fossil fuels is slowly killing our planet. Moreover, the cost of fossil fuel is also increasing day by day and its sources are gradually becoming exhausted. Therefore the use of fossil fuel is not a long-term solution to the prevalent power crisis in Bangladesh. As Bangladesh receives a lot of sunlight, therefore implementing a highly efficient and cost effective solar module can be an effective means to combat power crisis by producing large amounts of power at low cost.

In photovoltaic (PV) system, solar energy is converted into electrical energy through PV arrays. There are two mandatory tasks in a PV system (1) utilizing maximum energy from PV arrays. (2) Using the most reliable, highly efficient and cost effective configuration for the power converter to supply only pure sinusoidal current to the grid [1]. In conventional inverters, boost converters are used to step up the voltage at the output of the PV array to the grid voltage. Since a single-stage boost converter requires a high duty cycle which is inconvenient for MOSFET's switching; therefore a dual stage boost converter is used to get a duty cycle suitable for MOSFET switching. Also in conventional inverters, transformers are used to step down the grid voltage for frequency synchronization. But transformers are bulky, costly equipment contributing significantly to Total Harmonic Distortion (THD) of the output voltage [3]. In this paper, a transformer-less voltage divider circuit is employed to step down the grid voltage for frequency synchronization purposes. Further, unlike the conventional low pass LC filter, a T-LCL Immittance Converter is used at the output of the proposed inverter, which besides suppressing the harmonics also helps to maintain a constant output current. [4]

The proposed inverter consists of five main parts (1) A PV array for solar energy to electrical energy conversion. (2)A dual stage DC-DC boost converter to step-up PV array voltage to grid level. (3)An H-bridge DC-AC converter to obtain AC voltage. (4) A T-LCL Immitance converter to deliver a nearly constant and filtered current. (5) A transformer-less step-down AC-DC conversion circuit which is used to produce gate pulses for inverter switching by combining SPWM and square wave signals.

The block diagram of the proposed inverter configuration is shown below.

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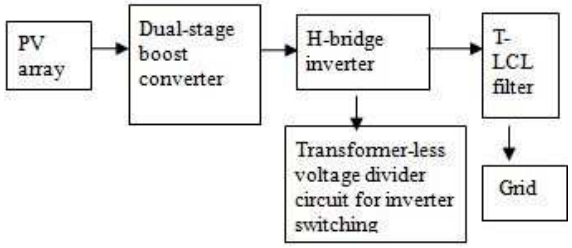

-1: Block diagram of inverter configuration

Design of Dual-Stage Boost Converter

In this section, the design of a dual stage DC-DC boost converter is presented which steps up the PV array voltage to a fixed high level grid voltage (312V peak or 220V rms in Bangladesh). In this paper, the dual stage (N=2) boost converter is proposed since the duty cycle of a single stage would be large (above 90%) which is not suitable for MOSFET's switching [6].The dual stage converter provides a more symmetrical duty cycle and reduces the voltage strain on the MOSFETs. Here the conversion is done based on the conversion ratio, x^2 =312/24 which converts 24V to 86V in the first stage and 86V to 312V in the second stage the design parameters of the first and second stages are listed in Table-I and Table-II respectively.

Table-1: Design of first stage boost converter

Symbol	Actual meaning	Value
V_{in}	Given input voltage	24V
V_{out}	Desired average output voltage	86V
f_s	Switching frequency of converter	20KHz
$I_{L,max}$	Maximum inductor current	260A
Δi_L	Estimated inductor ripple current(1.75% of $I_{L,max}$)	4.55A
ΔV_{out}	Desired output voltage ripple(0.05% of output voltage)	44mV
I_{out}	Maximum output current	4.3A

Table-2: Design of second stage boost converter

Symbol	Actual meaning	Value
V_{in}	Given input voltage	86V
V_{out}	Desired average output voltage	312V
f_s	Switching frequency of converter	21KHz
$I_{L,max}$	Maximum inductor current	230A
Δi_L	Estimated inductor ripple current(26% of $I_{L,max}$)	60A
ΔV_{out}	Desired output voltage ripple(0.1% of output voltage)	0.35V
I_{out}	Maximum output current	10.4A

Duty Cycle

Maximum duty cycle of first stage is,

$$D_1 = 1 - \frac{V_{in}}{V_{out}} = 1 - \frac{24}{86} \approx 0.72$$

Maximum duty cycle of second stage is,

$$D_2 = 1 - \frac{V_{in}}{V_{out}} = 1 - \frac{86}{312} \approx 0.72$$

Inductor Selection

The inductor values are selected using the following equation [7]

$$L = \frac{V_{in}(V_{out} - V_{in})}{I_L \times f_s \times V_{out}}$$

So, $L_1 = \frac{24 \times (86 - 24)}{4.55 \times 20000 \times 86} \approx 190\mu H$ and

$$L_2 = \frac{86 \times (312 - 86)}{60 \times 21000 \times 312} \approx 50\mu H$$

Capacitor Selection

The capacitor values are selected using the following equation [7]

$$C = \frac{I_{out} \times D}{f_s \times V_{out}}$$

So, $$C_1 = \frac{4.3 \times 0.72}{20000 \times 0.044} \approx 3.5mF$$

and

$$C_2 = \frac{10.4 \times 0.72}{21000 \times 0.35} \approx 1mF$$

The designed 24-312V DC-DC Boost Converter

The outputs of the first and second stages of the boost converter using PSIM simulation are shown in Fig2 and Fig3 respectively. The figures show that 24V has been boosted up to 312V.

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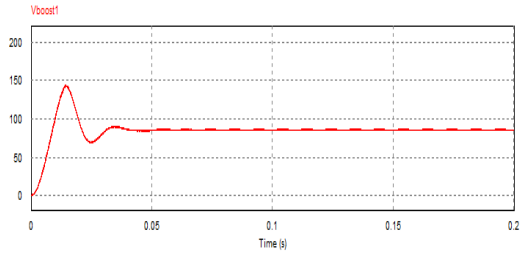

Fig-2: Boost converter output of the first stage

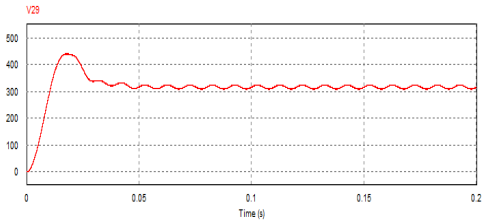

Fig-3: Boost converter output of the second stage

Design of the Transformer-Less Step down Circuit

The step down operation is performed using a voltage divider.

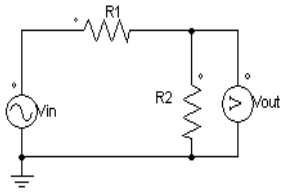

Fig-4: Voltage divider circuit

Using voltage divider equation, [7]

$$|v_{out}| = \frac{R2 \times |v_{in}|}{R1 + R2}$$

Setting

$|v_{in}| = 312\text{V}; |v_{out}| = 7.07\text{V}; R1 = 100\text{k}\Omega$ and solving for R2, we get R2=2.32KΩ.

The input voltage V_{in} (312Vpeak; 220V rms) and the output voltage V_{out} (7.07Vpeak; 5V rms) are shown in Fig 5 and Fig 6 respectively. The figures show that 312V has been stepped down to 7.07V.

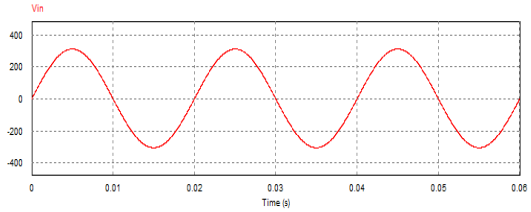

Fig-5: 312V peak (220V rms) input voltage

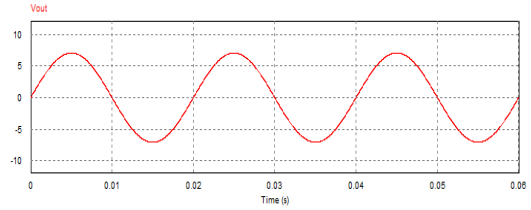

Fig-6: 7.07V peak (5V rms) output voltage

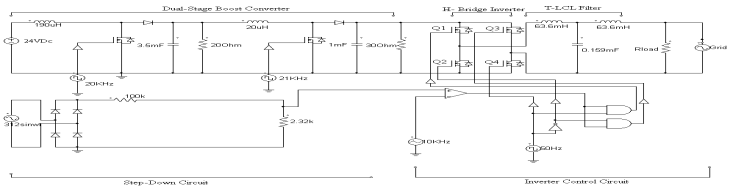

Fig-7: Proposed transformer-less grid-tie inverter

Proposed Grid-Tie Inverter Design

Grid Synchronization

The output voltage of a grid-tied inverter should maintain some fixed requirements so that it may provide power to grid [2]. The requirements are given below:

i. The amplitude of the output voltage should be equal to the amplitude of the grid voltage.
ii. The frequency of the inverter should be equal to the grid frequency (50Hz in Bangladesh).

In the proposed design, these conditions are achieved by sampling the grid frequency and using it to generate the switching signal. The GTI is connected to the power grid where the load is much higher as compared to the GTI. This means that the GTI has to force the power from the PV array into the grid. The real power is given by [2]

Real Power $P = \frac{|V_{inv}| \times |V_{grid}|}{Z_t} sin\ \phi$, where

Z_t= Linking line impedance
V_{inv}= Output voltage of inverter
V_{grid}= Grid voltage
ϕ= Angle between V_{inv} and V_{grid}.

From the above equation, it is clear that maximum real power can be transmitted into the grid for ϕ=90 degrees. If sinϕ is positive, then real power flows from the GTI into the grid; if sinϕ is negative, then real power follows in the reverse direction.

Power Circuits

The schematic circuit diagram of the proposed inverter is shown in Fig7. The DC-DC dual-stage boost converter steps up PV array voltage from 24V to 312V. The H-Bridge DC-AC inverter has two parallel MOSFET gates. A combination of analog and digital circuits is used to produce the gating pulses of the MOSFETs.

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Switching/Control Circuit

In conventional inverters only one type of switching technique is used. But this proposed design instead uses a combination of SPWM and square wave to reduce the switching loss by reducing the switching frequency. Fig 8 shows the proposed switching circuit of the GTI. The sine wave is sampled from the grid by using a transformer-less voltage divider circuit which steps down the voltage from 220V (rms) to 5V(rms).The sine wave sampled is used to generate the SPWM signal thus ensuring that the output voltage from the GTI will have the same frequency as the grid [5]. After sampling, the sine wave is rectified with a precision rectifier, the output of which is shown in Fig 9.

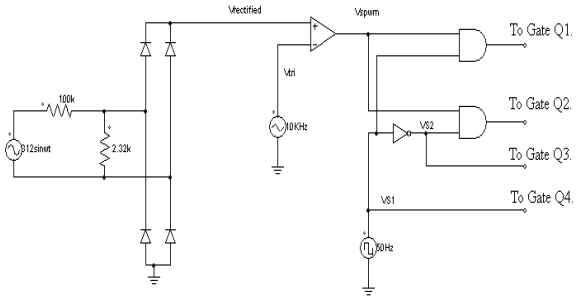

Fig-8: Control circuit of proposed GTI

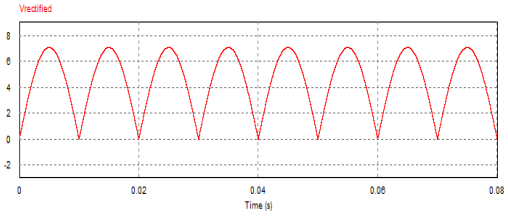

Fig-9: Rectified sine wave

In addition, a high frequency triangle wave of 10KHz is used. Then the two signals are passed through a comparator to produce the SPWM signal as shown in Fig 10. A square wave signal is used as the line frequency (50 Hz for Bangladesh) and is in phase with the SPWM as shown in Fig 11.The square wave is passed through a NOT gate to produce a signal that is 180 degree out of phase with the original signal.

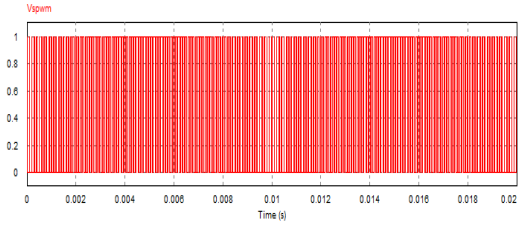

Fig-10: SPWM signal

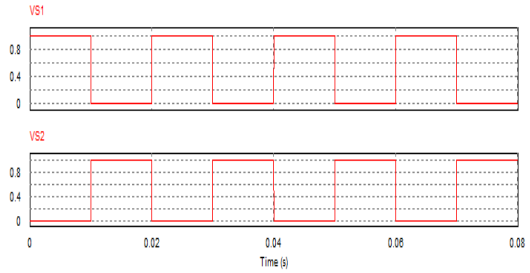

Fig-11: Square wave signals

The inverter requires four switching signals since it has four MOSFETs. To produce the four signals, an AND operation is performed between two sets of square wave signals and the SPWM signal. The four sets of switching signals can be categorized in two groups. The first group contains MOSFETs Q1 and Q4 while the second group contains MOSFETs Q2 and Q3. The gate pulses for switching of MOSFETs are illustrated in Figs 12 and 13 respectively. When Q4 is ON, Q1 is switched ON with the SPWM signal and both Q2 and Q3 are OFF. This produces a positive voltage at the inverter output. When Q3 is ON, Q2 is switched ON with the SPWM signal and Q1 and Q4 are both OFF. This produces a negative voltage at the inverter output.

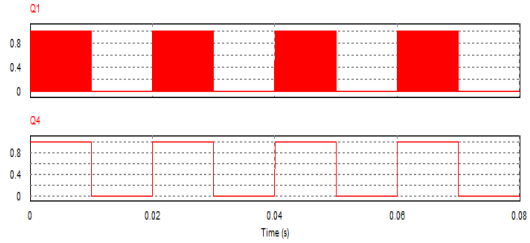

Fig-12: Switching signal from control circuit for MOSFETs (Q1 and Q4)

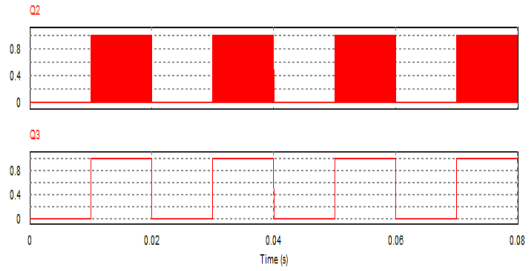

Fig-13: Switching signal from control circuit for MOSFETs (Q2 and Q3)

Filter Circuit

To eliminate harmonics from the inverter output, a filter circuit is employed. In conventional inverters, LC filter is used but this design employs a T-LCL Immitance Converter. The filter circuit consists of two inductors L_1 and L_2 and a capacitor C

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in the shape of a T as shown in Fig 7. From the derivation of the equation of the output current of the filter, I_2 is found as [4]:

$$I_2 \cong \frac{V_1}{Z_0}[1-\frac{Z_2}{QZ_0}].....(1)$$

Where V_1 is the input voltage, Z_2 is the load impedance and Q is the quality factor,

$$Q = \frac{\omega L}{r}.....(2)$$

With $\omega=2\pi f$ as the angular frequency, r is the internal resistance of the inductor and Z_0 is the characteristic impedance determined by L and C,

$$Z_0 = \sqrt{\frac{L}{C}} \quad ..... \qquad (3)$$

When *r* is negligible or zero, the quality factor becomes infinity. Under this condition,

$$I_2 = \frac{V_1}{Z_0}.....(4)$$

From eq. (4), it is observed that the output of the T-LCL filter is independent of load. Therefore this filter is capable of not only reducing harmonics but is also helpful in providing a constant current to the load.

The values of L and C of T-LCL filter (considering Butterworth type) is calculated using the cut-off frequency condition of low pass filters, i.e.

$$Z_0 = \frac{1}{2\pi f_c C}.....(5)$$ where Z_0 is the characteristic impedance given by Eq. (3). Assuming Z_0 as 20Ω and choosing f_c=50Hz, we get the values of L and C using Eqs. (3) and (5),

$$C = \frac{1}{2\times\pi\times 50\times 20} \approx 0.159\text{mF}$$

And L=C Z_0^2 =0.159 $\times 10^{-3} \times 20^2 \approx 63.60$mH

Power Transmitting

Voltage angle of GTI must lead grid voltage angle to transmit power into grid. To achieve this, the sampled sine wave from the grid is passed through a phase shifter circuit to make the leading adjustments. As mentioned earlier, to send maximum power into the grid, the leading angle must be 90 degrees. But in practice, due to stability reasons the angle is kept somewhat less than 90 degrees. [5]

Simulation Results

Inverter Output Voltage

Fig. 14 shows the output voltage waveform in the absence of any filter. The waveform is non-sinusoidal and contains lots of harmonics. To eliminate these harmonics, a low pass T-LCL filter is employed at the output of the inverter which produces a pure, sinusoidal voltage.

After filtering, we obtained a pure sinusoidal voltage of frequency 50Hz and of rms value 220V as shown in Fig 15.

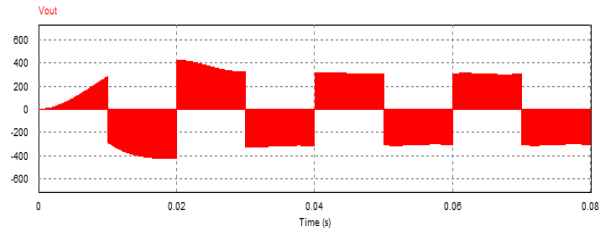

Fig-14: Output voltage without filtering in PSIM.

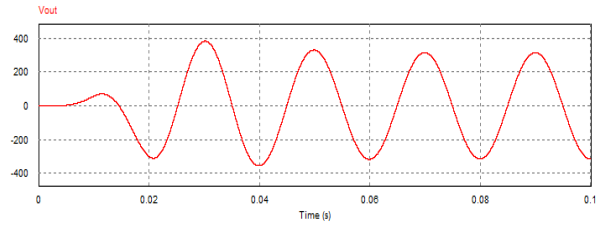

Fig-15: Output voltage after filtering in PSIM

Inverter Output Current

The peak value of the inverter output current is an important factor in designing the inverter stack size. The inverter current rating is normally determined by the filter impedance and the rated load impedance in a steady-state. Fig. 16 shows the output current.

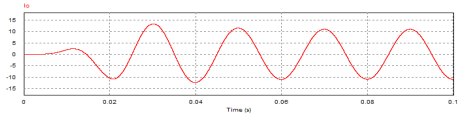

Fig-16: Output current waveform in PSIM

In order to test the performance of the inverter, the load current was measured for both R and RL load with and without using the filter circuit. The load impedance was varied from 5Ω to100Ω for both R and RL load by considering the characteristic impedance as Z_0=20Ω. It was observed that the load current without filter varies in a large range than the current with the filter circuit employed as shown in Fig 17. It is also observed that the load current for both resistive and inductive load remains almost constant which confirms that the output current is nearly independent of load for a T-LCL filter.

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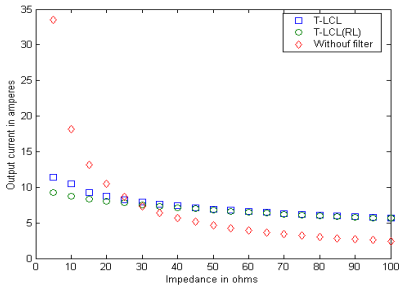

Fig-17: Output current vs. load impedance

Inverter Efficiency

The inverter efficiency is calculated using the following formula:

$$\eta = \frac{P_{out}}{P_{in}} \times 100\% \ldots\ldots. (6)$$

where P_{in} and P_{out} are the input and output powers of the inverter respectively. By varying the load impedance, the inverter efficiency was measured for the T-LCL filter as shown in Fig 19. The graph shows that the inverter efficiency is over 90% for the entire load range with a peak value of nearly 97%.

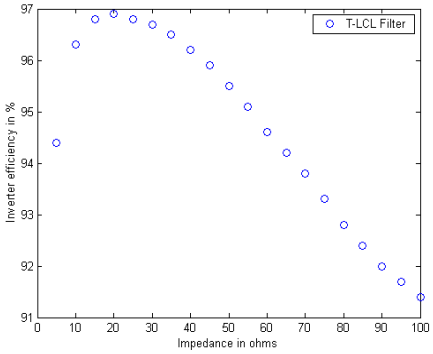

Fig-18: Efficiency vs. load impedance

Conclusions

This paper presents a transformer-less PV grid-tie inverter for residential application, the output of which is 220V rms at a frequency of 50Hz. The PSIM simulation results confirm these. The power loss in the transformer-less circuit is only 473mW which is much less than the loss incurred with a transformer. The total harmonic distortion of the output voltage is 0.1% which is much lower than the IEEE 519 standard and the efficiency of the inverter swells up to 97%. Therefore the proposed inverter design is highly efficient, cost-effective and compact due to being transformer-less and provides a near constant current which ensures stability.

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